What is claimed is:

1. A semiconductor package, comprising:

a substrate having a resin layer with first and second surfaces wherein a plurality of electrically conductive patterns are formed thereon, the resin layer having an aperture formed at the center thereof;

a first semiconductor chip having first and second surfaces, the second surface having a plurality of input/output pads formed thereon, the first semiconductor chip being placed in the aperture of the substrate;

a plurality of first conductive wires for connecting the input/output pads of the first semiconductor chip to the electrically conductive patterns formed on the second surface of the resin layer of the substrate;

an adhesive attached to the second surface of the first semiconductor chip;

a second semiconductor chip having first and second surfaces, the second surface having a plurality of input/output pads formed thereon, the second semiconductor chip being attached to the adhesive;

a plurality of second conductive wires for connecting the input/output pads of the second semiconductor chip to the electrically conductive patterns formed on the second surface of the resin layer of the substrate;

an encapsulate for encapsulating up the aperture of the substrate, the first and second semiconductor chips, and the first and second conductive wires; and

a plurality of conductive balls coupled to the electrically conductive patterns formed on the second surface of the resin layer of the substrate.

2. The semiconductor package in accordance with Claim 1 wherein each of first conductive wires for connecting the input/output pads of the first semiconductor chip to the electrically conductive patterns formed on the second surface of the resin layer of the substrate are stand off stitch bonded.

3. The semiconductor package in accordance with Claim 1 wherein one end of each first conductive wire is ball-bonded to one of the electrically conductive patterns and the other end is stitch-bonded to one of the input/output pads of the first semiconductor chip so that the maximum curved portion of the first conductive wire is placed on the electrically conductive pattern.

4. The semiconductor package in accordance with Claim 3 wherein a conductive ball is coupled to the input/output pad of the first semiconductor chip and the first conductive wire is stitch-bonded to the conductive ball.

5. The semiconductor package in accordance with Claim 3 wherein each of the plurality of second conductive wires for connecting the input/output pads of the second semiconductor chip to the electrically conductive patterns formed on the second surface of the resin layer of the substrate are normal wire bonded.

6. The semiconductor package in accordance with Claim 3 wherein one end of each second conductive wire is ball-bonded to one of the electrically conductive patterns and the other end is stitch-bonded to one of the input/output pads of the second semiconductor chip so that the maximum curved portion of the second conductive wire is placed on the electrically conductive pattern.

7. The semiconductor package in accordance with Claim 6 wherein a conductive ball is fused to the input/output pad of the second semiconductor chip and the second conductive wire is stitch-bonded to the conductive ball.

8. The semiconductor package in accordance with Claim 1 further comprising a plate-shaped conductive thin film formed on the first surface of the first semiconductor chip, the conductive thin film being extended to the encapsulated portion around the first semiconductor chip and the substrate.

9. The semiconductor package in accordance with Claim 8 wherein the electrically conductive patterns are formed on the first and second surfaces of the resin layer through a conductive via.

10. The semiconductor package in accordance with Claim 9 wherein the electrically conductive patterns formed on the second surface of the resin layer are electrically connected to the conductive thin film.

11. The semiconductor package in accordance with Claim 1 wherein the adhesive is silicon having an adhesive layer formed on a top and bottom surface of the thereon.

12. The semiconductor package in accordance with Claim 1 wherein the second semiconductor chip has an insulating layer formed on the first surface thereof.

13. The semiconductor package in accordance with Claim 1 wherein the horizontal width of the second semiconductor chip is wider than that of the first semiconductor chip.

14. A semiconductor package, comprising:

a substrate having a resin layer with first and second surfaces wherein a plurality of electrically conductive patterns are formed thereon, the resin layer having an aperture formed at the center thereof;

a first semiconductor chip having first and second surfaces, the second surface having a plurality of input/output pads formed thereon, the first semiconductor chip being placed in the aperture of the substrate;

a plurality of first conductive wires for connecting the input/output pads of the fir semiconductor chip to the electrically conductive patterns formed on the second surface of the resin layer of the substrate;

a second semiconductor chip having first and second surfaces, the second surface having a plurality of input/output pads formed thereon;

means coupled to the second surface of the first semiconductor chip for coupling the first semiconductor chip to the second semiconductor chip;

a plurality of second conductive wires for connecting the input/output pads of the second semiconductor chip to the electrically conductive patterns formed on the second surface of the resin layer of the substrate;

means for encapsulating up the aperture of the substrate, the first and second semiconductor chips, and the first and second conductive wires; and

a plurality of conductive balls coupled to the electrically conductive patterns formed on the second surface of the resin layer of the substrate.

15. The semiconductor package in accordance with Claim 14 wherein one end of each first conductive wire is ball-bonded to one of the electrically conductive patterns and the other end is stitch-bonded to one of the input/output pads of the first semiconductor chip so that the maximum curved portion of the first conductive wire is placed on the electrically conductive pattern.

16. The semiconductor package in accordance with Claim 14 wherein one end of each second conductive wire is ball-bonded to one of the electrically conductive patterns and the other end is stitch-bonded to one of the input/output pads of the second semiconductor chip so that the maximum curved portion of the second conductive wire is placed on the electrically conductive pattern.

17. The semiconductor package in accordance with Claim 14 further comprising a plate-shaped conductive thin film formed on the first surface of the first semiconductor chip, the conductive thin film being extended to the encapsulated portion around the first semiconductor chip and the substrate.

18. The semiconductor package in accordance with Claim 17 wherein the electrically conductive patterns formed on the second surface of the resin layer are electrically connected to the conductive thin film.

19. The semiconductor package in accordance with Claim 14 wherein the second semiconductor chip has an insulating layer formed on the first surface thereof.

20. A method of forming a semiconductor package comprising:

providing a substrate having a resin layer with first and second surfaces wherein plurality of electrically conductive patterns are formed thereon, the resin layer having an aperture formed at the center thereof;

covering the aperture with an adhesive tape;

attaching a first semiconductor chip to the adhesive tape;

coupling a plurality of first conductive wires to input/output pads of the first semiconductor chip and to the electrically conductive patterns formed on the second surface of the resin layer of the substrate;

attaching an adhesive layer to the second surface of the first semiconductor chip;

coupling a second semiconductor chip to the adhesive layer;

coupling a plurality of second conductive wires to input/output pads of the second semiconductor chip and to the electrically conductive patterns formed on the second surface of the resin layer of the substrate;

encapsulating the aperture of the substrate, the first and second semiconductor chips, and the first and second conductive wires; and

coupling a plurality of conductive balls to the electrically conductive patterns formed on the second surface of the resin layer of the substrate.

21. The method of Claim 20 further comprising:

ball bonding one end of each first conductive wire to one of the electrically conductive patterns; and

stitch-bonding a second end of each first conductive wire to one of the input/output pads of the first semiconductor chip so that the maximum curved portion of the first conductive wire is placed on the electrically conductive pattern.

22. The method of Claim 20 further comprising:

ball bonding one end of each second conductive wire to one of the electrically conductive patterns; and

stitch-bonding another end of the second conductive wire to one of the input/output pads of the second semiconductor chip so that the maximum curved portion of the second conductive wire is placed on the electrically conductive pattern.

23. The method of Claim 22 further comprising:

coupling a conductive ball to the input/output pad of the second semiconductor chip; and

stitch bonding the second conductive wire to the conductive ball.

24. The method of Claim 20 further comprising coupling a plate-shaped conductive thin film formed on the first surface of the first semiconductor chip, the conductive thin film being extended to the encapsulated portion around the first semiconductor chip and the substrate.

25. The method of Claim 24 further comprising coupling the electrically conductive patterns formed on the second surface of the resin layer to the conductive thin film.

26. The method of Claim 20 further comprising forming an insulating layer on the first surface of the second semiconductor chip.